Capacitance Meter – Final Report

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Discussion

Summary of our Device

To measure capacitance, our device takes advantage of an element law of capacitors: $I = C(dV/dt)$. By passing an oscillating voltage through the capacitor and using a trans-impedance amp, we find the current through the capacitor. This current is output as a voltage. To 'freeze' the derivative to a single value and thus make our current-to-capacitance relation linear, we use a peak detector. The precision peak detector outputs the peak current through the capacitor as a voltage. As our measurement is of a single point in the voltage period, and the period of the change in voltage across the capacitor about time has the same period, there is a single point in the dV/dt period corresponding to our measured point. As this single point has a constant value, the output of the peak detector is directly proportional to capacitance.

To measure capacitance about three decades while only outputting in the 0.5 V to 5 V range, we split our capacitance output ranges into three decades: 5 nF - 50 nF, 50 nF - 500 nF, 500 nF - 5 μF. Each decade would output between 0.5 V to 5 V. To accomplish this, we apply a 1/10th gain to the output for capacitance values in the middle decade (50 nF - 500 nF), and a 1/100th gain to the output for capacitance values in the upper decade (500 nF - 5 μF).

To accomplish the three levels of gain, 1x, 1/10x, and 1/100x, we used two 2 Vpp Wein Bridge oscillators of ω = 10k (rad/s) and ω = 1k (rad/s), respectively, and an inverting amplifier of 10x gain. Switching between these two oscillators affords a 1/10x gain to the output. This works because we measure current through the capacitor, and the current through the capacitor is capacitance times the derivative of the voltage across the capacitor, and the derivative of voltage is proportional to the angular frequency. So, using the ω = 10k oscillator, then switching to the ω = 1k oscillator with 1/10th the angular frequency, we apply a 1/10x gain to our output. To accomplish a 1/100x gain, we create a second 1/10x gain module that we place in series Wein Bridge oscillators. This second 1/10th gain module is constructed by reading the output of the TIA directly (1x gain) or through a 10x inverting amplifier (10x gain). By initially reading the output of the 10x inverting amplifier and then switching to the output of the TIA directly, we create a 1/10x gain.

To decide which Wein Bridge oscillator to use and whether to read the signal directly from the TIA or from the 10x inverting amplifier, we used digital logic. Our components are a comparator, a MUX, two SR latches, a NAND gate, a NOT gate, a 3V DC step-up, a 3V DC step-down, an RC delay, and an RC lowpass filter. The output of both oscillators and both outputs of the TIA are imputed into the MUX. The two oscillator MUX outputs are connected to a single wire and controlled by one SR latch. The two TIA outputs of the MUX are also connected by a single wire and controlled by the second SR latch. This results in the MUX outputting one oscillator or the other at a time and one TIA output or the other at a time.

Our logic begins with the assumption that the capacitor placed is in our lowest decade, 5 nF - 50 nF, and that the reset button has been hit, setting the SR latch outputs to Q = 0 and Q' = 1. Both Wein Bridge

oscillator signals flow through a 3V DC step-up, resulting in a positive signal oscillating between 3 and 5 volts. This is necessary, as the MUX can only pass positive signals. Q' on the second SR latch beings at a digital 1, which lets the Wein Bridge of ω = 10k pass through the MUX. At the same time, the Wein Bridge of ω = 1k is blocked by the output of Q on the second SR latch being 0. Thus, only the larger angular frequency oscillator signal passes through the MUX. This signal is fed through a 3V step down, before flowing through the DUT and the TIA.

The output of the TIA is fed directly back into the MUX, or passes through a 10x inverting amplifier and a low pass filter before inputting into the MUX. The purpose of the low pass filter is to reduce noise on the peak of the signal, which starts as noise at the bottom of the TIA output signal that becomes noise at the peak of the 10x inverting amplifier output. Because we assume the capacitor under test is of the lowest decade, Q' of the first SR latch allows the 10x gain signal to pass, while Q of the first SR latch blocks the 1x gain signal. The 10x gain signal then passes through a precision peak detector with a large time constant to hold output voltages steady. Because we are concerned with the positive peak output signal and none of the negative signal, we do not have to add the 3V step up and down around the MUX for the TIA signals. Finally, the output of the peak detector is read as the output of the capacitance meter.

In series with this output, however, is a comparator with a threshold voltage of 5.35 Volts. If the output signal is larger than 5 volts, we know the capacitance of the DUT must be either in the middle or high decade and thus, the comparator outputs a signal to the first SR latch. This sets the SR latch, its Q to output a signal, and its Q' to stop its signal. As this SR latch is tied to the output of the TIA, setting this SR latch causes the MUX to output the 1x TIA signal instead of the 10x TIA signal, obtaining 1/10x gain. This signal again goes to the peak detector, where the capacitance value is outputted. To note, the setting of the first SR latch turns on an LED, allowing a user to know the value is in the middle decade.

If, however, the output is still larger than 5 volts, we know it must be in the highest decade. To sense this, the output of the comparator and Q of the first SR latch are connected to a NAND gate in series with a NOT gate. Additionally, a RC delay circuit sits between the Q of the first SR latch and the NAND gate. The logic is, if the capacitance is in the middle decade, the comparator will briefly input a signal before stopping once the TIA output through the MUX shifts. The Q of the first SR latch will also send a signal that is delayed by the RC delay. Thus, if the device is in the second decade, the comparator will stop outputting a digital one before the Q of the first SR latch inputs a digital one; however, if the DUT is in the final decade, both the comparator and Q of the first SR latch input a digital one into the NAND-NOT gate pair, which outputs a digital one to a second SR latch. Triggering this SR latch causes the Wein Bridge input to switch from high to low angular frequency. The resulting 1/10x gain in series with the TIA output 1/10x gain results in a total gain of 1/100x. This low angular frequency signal then flows through the DUT and TIA, into the MUX without the 10x gain as the first SR latch is set, into the peak detector, where the output shows the capacitance. Additionally, a second LED lights up when the second SR latch is set, letting users know the output value is in the highest decade.

In the end, our device works well as a qualitative estimate of a capacitance value. As seen in the performance section, of the 11 capacitors tested, our device correctly outputted the capacitance within 5% for 7 with the largest error being 8.2%. The average percent error from our experiments was 3%, well within the specifications. Furthermore, since we did not have access to an actual capacitance meter, the

values we compared our results to was the ideal value on the capacitor; therefore, another error source could have been a discrepancy between the written value and the actual capacitance–it is impossible to blame the error wholly on our meter. In terms of user flow, our device is simple to use: you hit the reset button, place the capacitor you would like to test, and read the output voltage of the peak detector while noting how many LEDs are lit up. Capacitance values are found almost instantaneously on a human scale when capacitors are placed.

Design Methodology

Our design methodology closely resembled the flow of the three phases: first, we created a high-level block diagram, then we made the circuit in an LTSpice simulation. Next, we tried to use the components we had in the lab, and then we finally created the actual circuit in the lab on a breadboard. Throughout the process, we either incorporated feedback from the teaching staff or from testing our circuit in the sim or on the board. This process worked well for our group as we were gradually nudged toward the optimal design. At the beginning of the project, it was tempting to skip past the block diagram phase straight to simulation. Still, we found this jump distracting from figuring out how each component interacted with each other at a high level. If we were to do the same project or a similar project again, it would make the most sense to follow this same process.

Changes made in our circuit design in Phase 3.

Most of the changes we made during phase 3 were regarding digital logic. Because the specific quad switch component was not available in LTSpice, we didn't completely flesh out the interaction between the analog and digital components. One key change was adding an RC delay on the node between Q1 and the NAND gate. This delay was important for measuring the second decade of capacitance values, otherwise the logic would immediately force through to the third decade. The delay was measured on the oscilloscope to be around ~5 ms.

In addition to changes related directly to circuit logic, we made changes to our Wein Bridge oscillators due to the specifications of our MUX chip. The MUX in the lab can only handle positive signals as inputs, so to make our Wein Bridge compatible, we added a 3v DC offset to our oscillator signal before entering the MUX and removed said offset before the signal passed through the DUT.

Another change was adding a passive low-pass filter after the 10x inverting amplifier. This was added after observing high-frequency noise near the peaks of our TIA/gain amplifier output. The noise frequency was around 180-220 kHz and so we set the cut-off frequency at ~50 kHz since the peak input Weinbridge frequency was only 1.569 kHz.

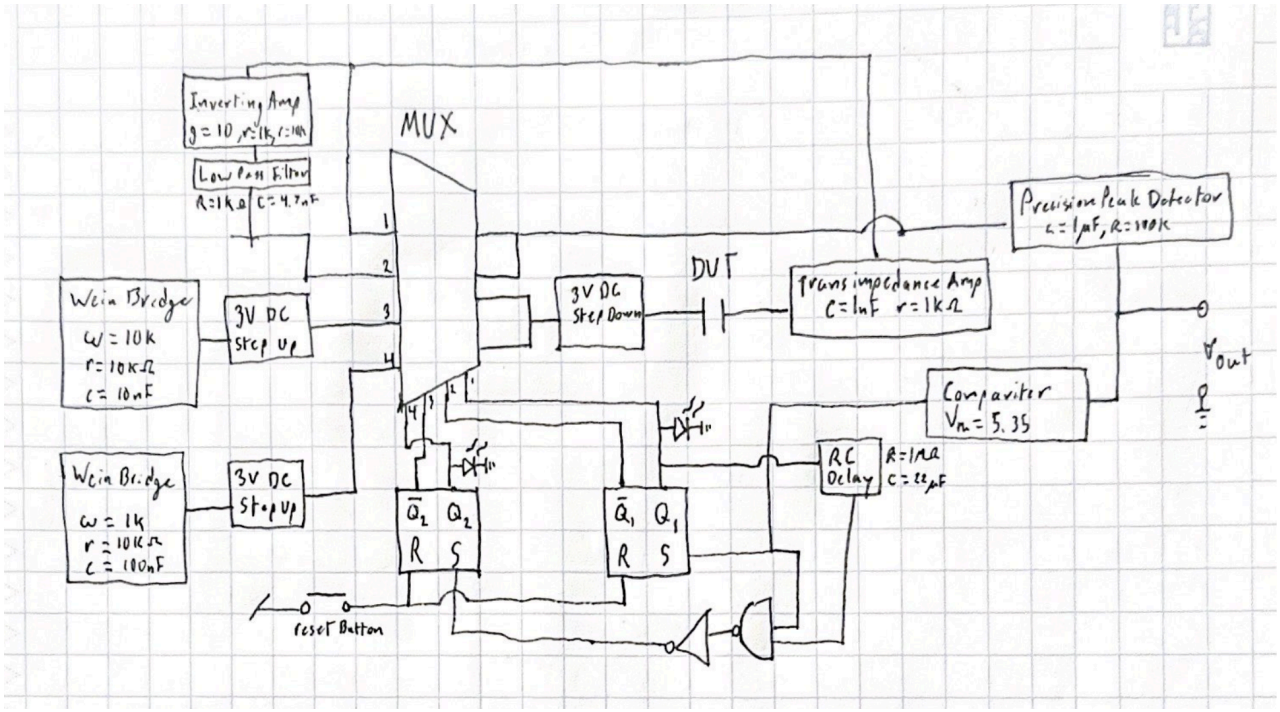
Also, we changed the V_{thresh} value on the comparator to 5.35 volts so that it would trigger sooner.

Debugging techniques, challenges encountered, and lessons learned.

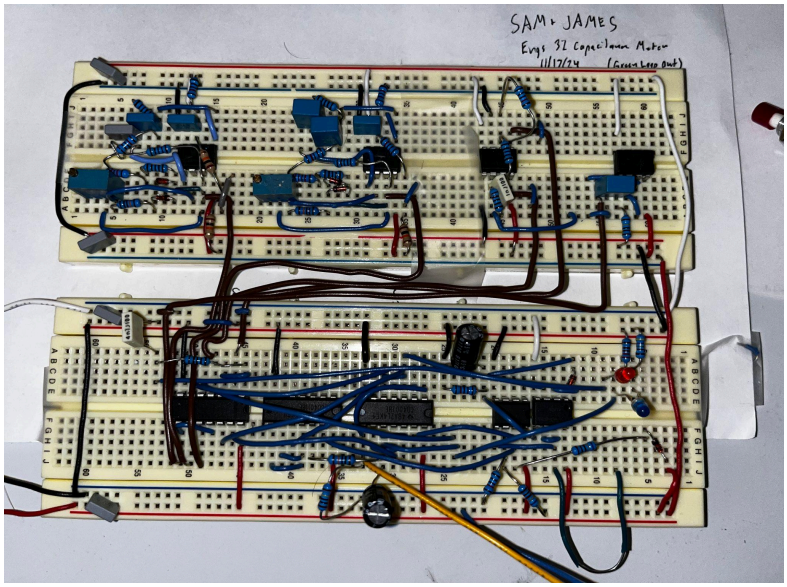
We did extensive unit tests on the components labeled in our block diagram before combining them. This process was constructive for isolating issues in our circuit before the complexity got out of control. In particular, testing the digital logic with a voltmeter proved super effective in identifying bugs with SR latches and the comparator.

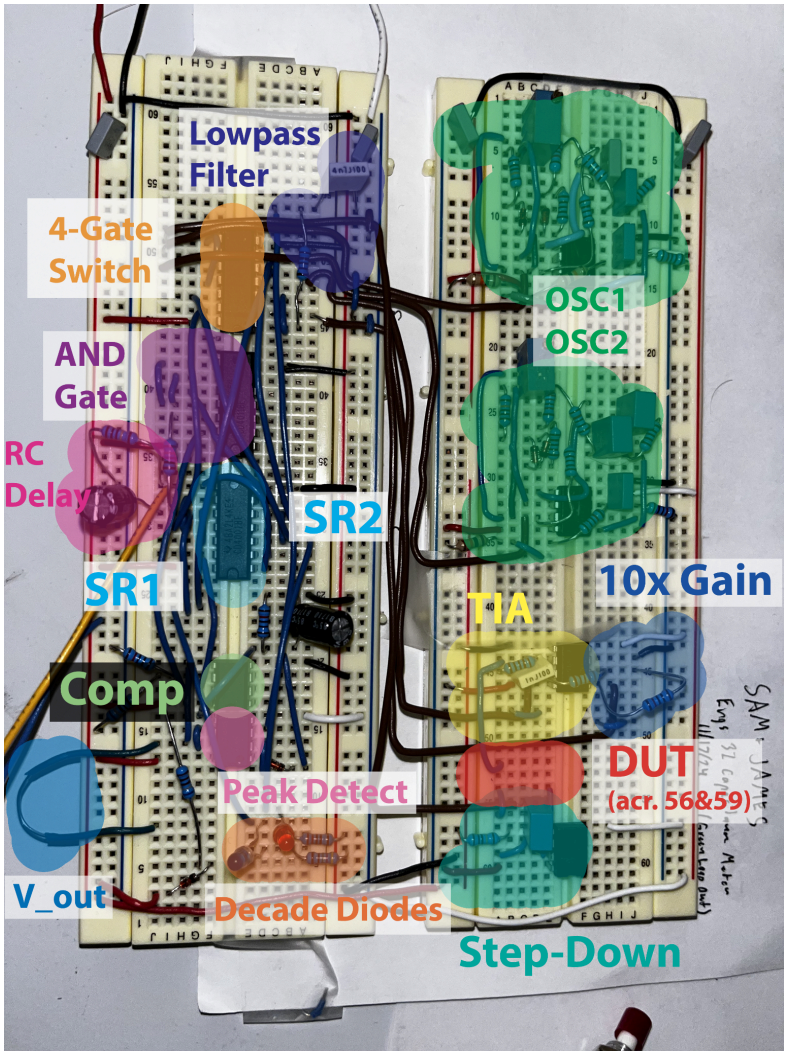
Documentation

Block Diagram

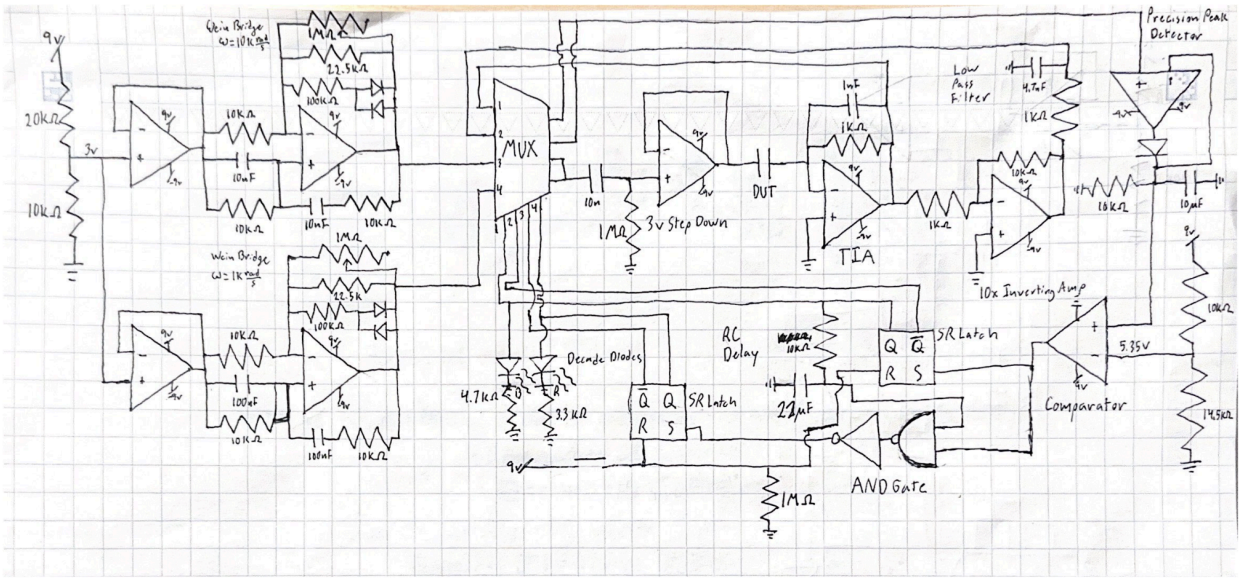


Breadboard


SAM + JAMES


Lowpass Filter
4-Gate Switch
AND Gate
RC Delay
SR2
SR1
Comp
V_out
Peak Detect
Decade Diodes
OSC1
OSC2
TIA
10x Gain
DUT
(acr. 56&59)
Step-Down

Schematic



Circuit specifications

DC 3V Step up • R1 = 20 kΩ • R2 = 10 kΩ	Oscillator 1: F = 1.62 kHz, V_{PP} = 2.06 V • Rosc= 10 kΩ • Cosc= 10 nF	Oscillator 2: F = 156.48 Hz, V_{PP} = 2.03 V • Rosc = 10kΩ • Cosc = 100nF	Step Down • R = 1MΩ • C = 1 μF
TIA • R = 1 kΩ • C = 1 nF	Inverting Amp • Rf = 10 kΩ • Rin = 1 kΩ	Low Pass Filter • R = 1 kΩ • C = 4.7 nF	Peak Detector • τ = 100 ms • R=10 kΩ • C=10 μF
Comparator • V_{thresh} = 5.35 V	Logic Components • V_{high} = 9 V • V_{low} = 0 V • V_{thresh} = 4.5 V	Delay on SR Output to NAND Gate • R = 10 kΩ • C = 22 μF	Decade Diodes • Rred = 3.3 kΩ • Rblue = 4.7 kΩ

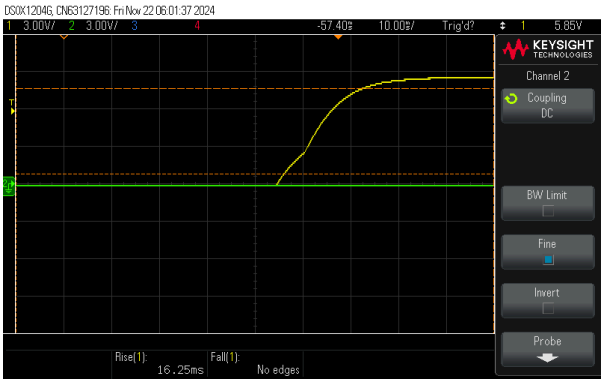
Circuit descriptions

Reset Button

The reset button resets the state of the SR latches, setting them both to zero, to allow the capacitance meter to start looking at the lowest decade of capacitance again. We tied the positive side of the button to +9 V, the negative side to the reset pins, and branching to ground through a 1 MΩ resistor. The resistor limits current, preventing the button from shorting the power rails, but still provides ~9V to the reset pins when it is pressed.

AND Gate

We used two NAND gates out of the four provided on the chip. The first NAND gate is used simply as a NAND gate between a delayed Q1, and the comparator. The second NAND gate is used as an inverter before feeding to the set pin of SR2. The RC delay, mentioned earlier, prevents the circuit from switching past the second decade for second-decade capacitors. The values chosen (10 kΩ & 22 µF) should provide a delay of 220 ms, but we saw a delay of 16 ms instead on the oscilloscope. However, this delay proved to be enough.



RC Delay

Peak Detect

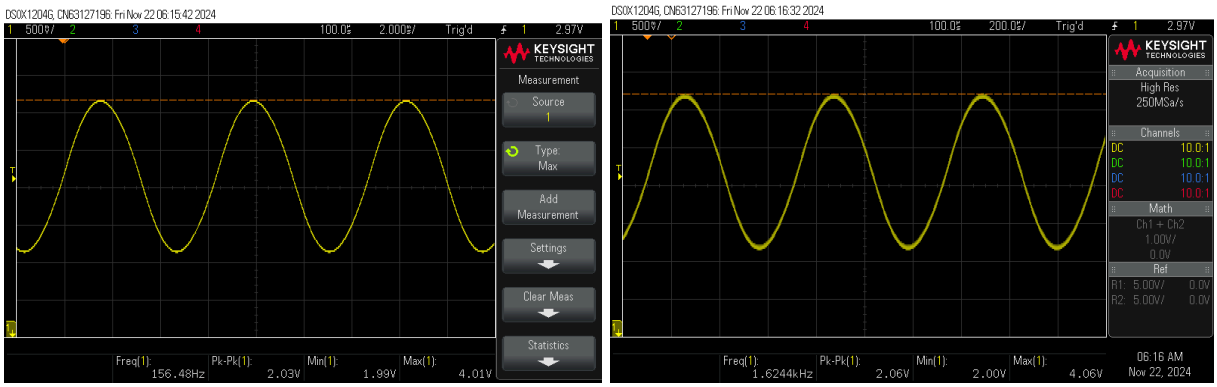
We use a simple peak detect circuit that we learned in class, consisting of a diode and RC components. The RC values were 10 kΩ and 10 µF, and were chosen for a smooth DC-like signal with a RC time constant of 100 ms.

10x Gain

We use a simple inverting op-amp setup with resistor values of 10 kΩ and 1 kΩ. Switching from a signal through this inverting amplifier to the signal directly is one of the two ways we apply a 1/10th gain on the circuit when switching between decades.

Oscillators

We used two weinbridge oscillators to send a sine wave into our circuit. Using R = 10 kΩ and C = 10 nF we set one oscillator to an angular frequency of 10k rad/s, and R = 10 kΩ with C = 100 nF for a second oscillator with an angular frequency of 1k rad/s. To create a peak-to-peak amplitude of two volts, we used a tunable resistor in parallel with a 22.5 kΩ and 100 kΩ resistor, with both oscillators individually tuned.



Weinbridge Oscillators

Step up and Step down

Because the MAX4066 can only pass positive signals, we use a 10 kΩ and 20kΩ resistor divider feeding into a buffer, which feeds into the ‘ground’ nodes for the weinbridge oscillator to give the weinbridge output a 3V DC offset. This causes our weinbridge waveform to oscillate between 3V and 5V, which the MAX4066 can handle. However, before the signal passes through the DUT, it must be offset back to zero volts. The step down with a C = 1 µF and R = 1 MΩ right before the DUT does just this to the oscillator signal.

Comparator

We used an op-amp comparator with a negative input of 5.35 volts, achieved through a voltage divider off the power rails. This allows the circuit to ‘see’ if the signal is above 5.35 volts and, therefore, if a 1/10th gain should be applied. If a capacitance is above 53.5 nF, the capacitor will fire to apply a 1/10th gain to the signal by switching the TIA output of the MUX. If the capacitance is above 535 nF the comparator will fire a second time, causing a second 1/10th gain to be applied to the circuit for a total gain of 1/100 on the signal.

RC Delay

The NAND-NOT gate is tied to the Q of the first SR latch and the output of the comparator. However, Q of the first SR latch is also tied to the output of the comparator. This means when the comparator outputs a signal, both inputs to the NAND-NOT gate are a digital one, resulting in a

SR Latches

We use the quad NOR-gate chip which perfectly fits two SR latches. Both reset pins are tied to the push-button such that the SR latches reset to 0 when the button is pressed. The output of SR1 is tied to the RC delay circuit mentioned above.

MUX

We are using the MAX4066 analog switch as a four-gate multiplexer to use digital logic to select elements of our circuit. The first two gates are controlled by Q1' and Q1 respectively to select either 10x or 1x gain, and the second two gates are controlled by Q2' and Q2 respectively, selecting either high or low frequency oscillation. Since the MAX4066 chip cannot pass negative voltages, the input oscillations are DC-shifted up by 3 V. We only care about the positive peaks on the output of the TIA, so there is no need for this level-shift on those inputs.

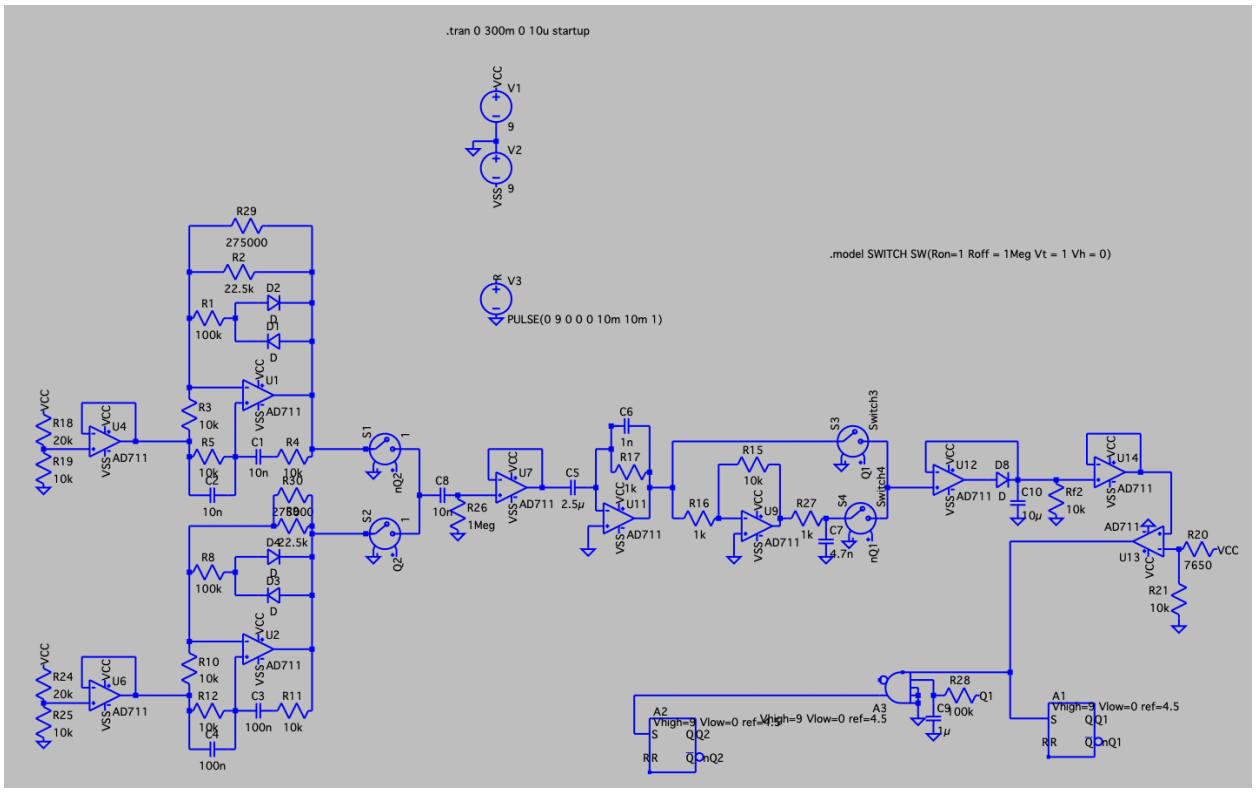
TIA

The trans-impedance amplifier uses a 1 kΩ resistor and 1 nF capacitor. With these RC values, it has a gain of 1000 from A->V, and has an upper cutoff frequency of 159 kHz.

Lowpass Filter

We put a low-pass filter on the input of the peak detector to prevent an overshoot of the desired voltage. We used RC values of 1 kΩ & 4.7 nF, correlating with a cutoff frequency of ~34 kHz which is well above our high-frequency oscillations. Although it smoothed out our oscilloscope readout after the filter, it did not actually affect the output voltage much after it passed through the peak detector.

Simulation results using the components and values from the final device.



Full Circuit simulations come from the above LTSpice circuit

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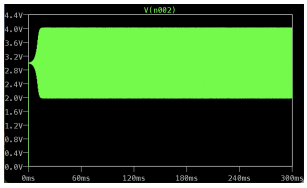
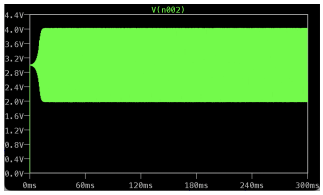
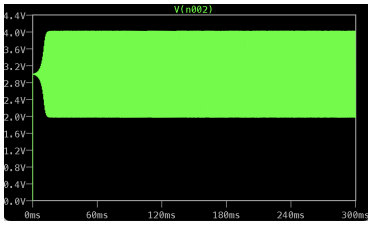
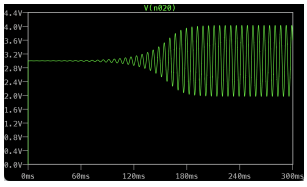
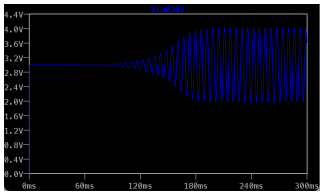
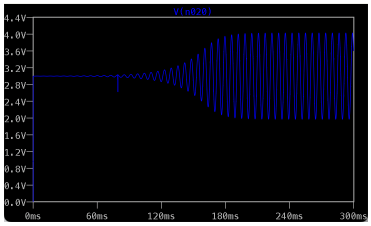
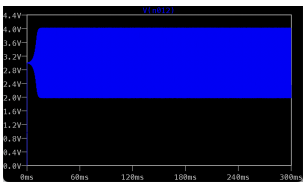
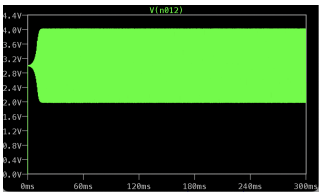
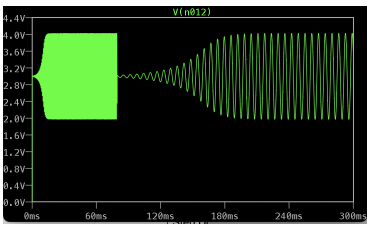
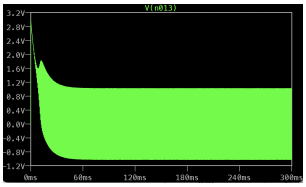
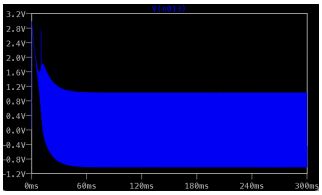
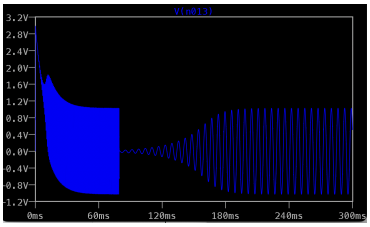
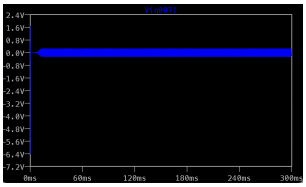
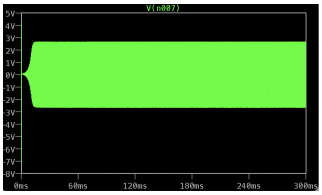
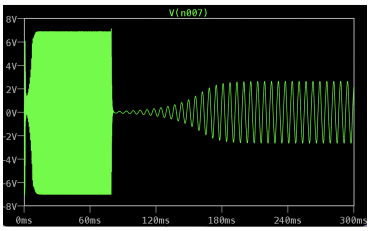
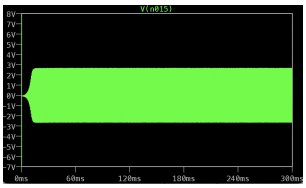
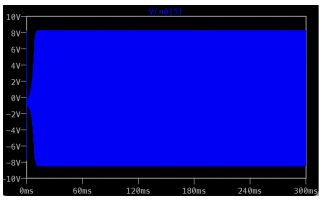
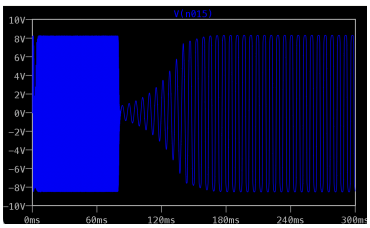
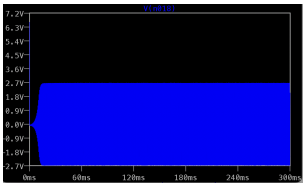
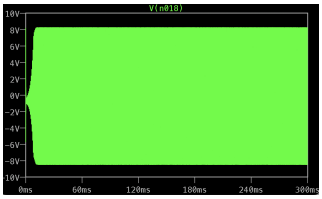
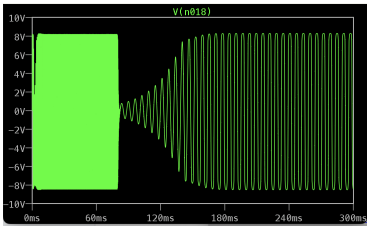
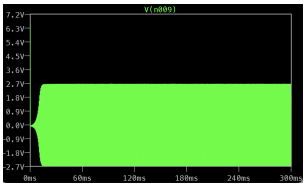
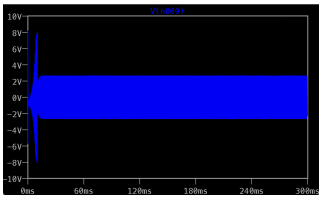
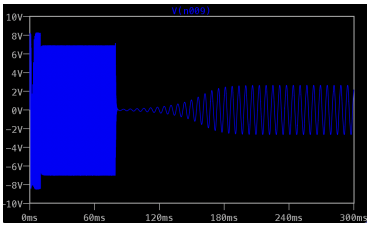
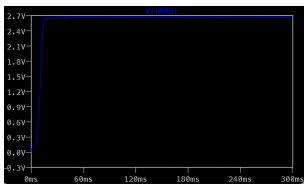
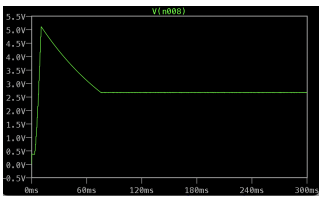
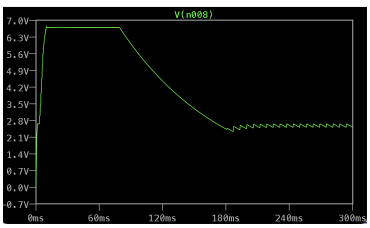
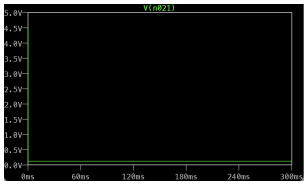
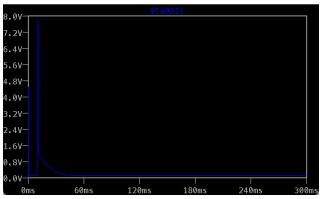
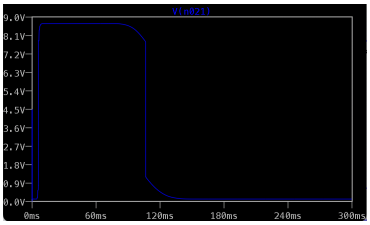
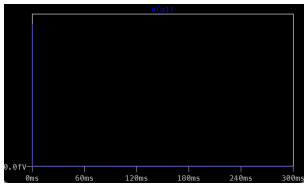
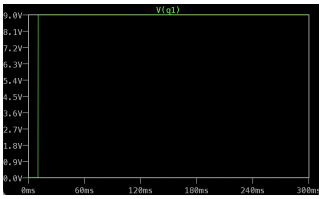
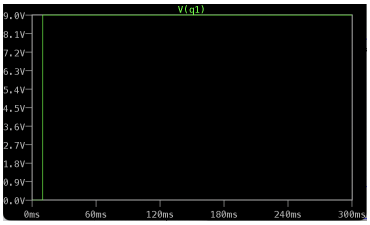
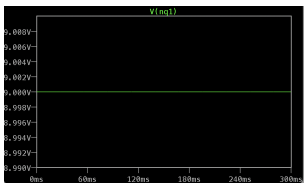
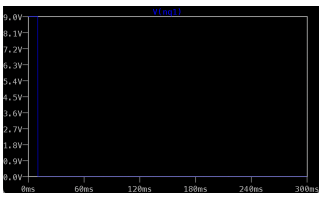
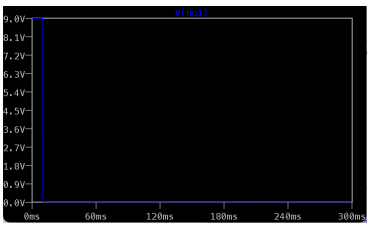
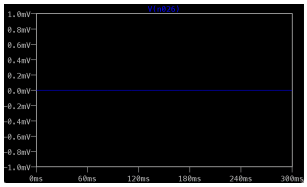
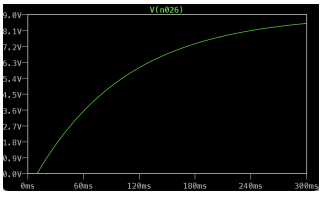
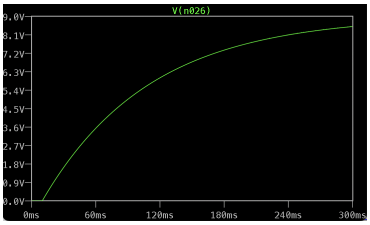
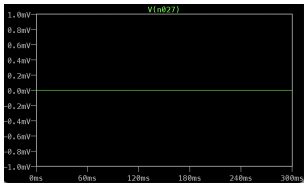
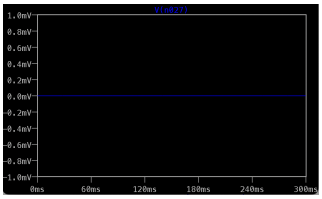
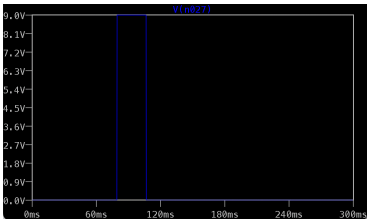
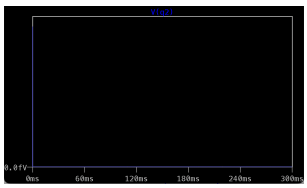
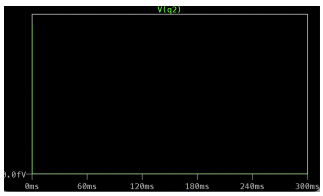
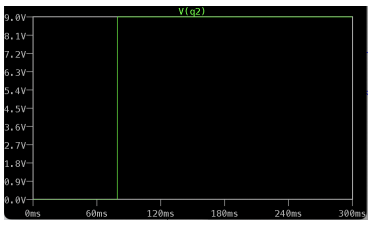
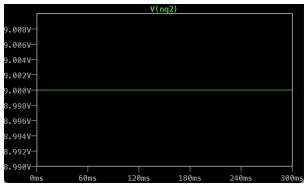
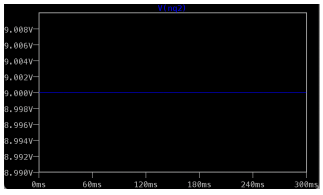
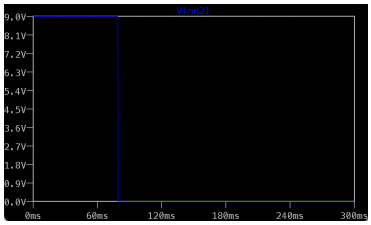
Wein Bridge w=10k			
Wein Bridge w=1k			

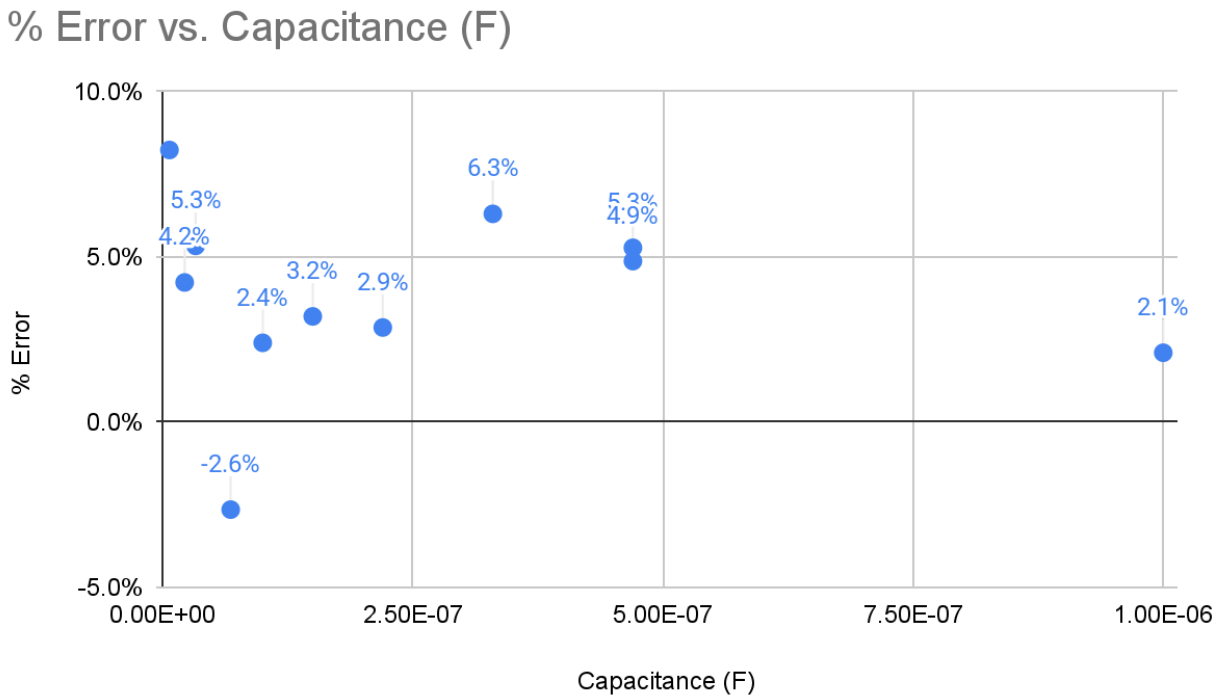
MUX Osc out			
Step Down			
TIA			
10x Inverting Amp			
Low Pass Filter			
MUX TIA out			

Precision Peak Detector			
Comparator			
Q1			
Q1’			
RC Delay			
NAND-NOT			

Q2			
Q2’			

Performance

Capacitance (F)	Expected Output (V)	Actual Output (V)	% Error
6.80E-09	0.680	0.736	8.2%
2.20E-08	2.200	2.293	4.2%
3.30E-08	3.300	3.476	5.3%
6.80E-08	0.680	0.662	-2.6%
1.00E-07	1.000	1.024	2.4%
1.50E-07	1.500	1.548	3.2%
2.20E-07	2.200	2.263	2.9%
3.30E-07	3.300	3.508	6.3%
4.70E-07	4.700	4.948	5.3%
1.00E-06	1.000	1.021	2.1%
4.70E-07	4.700	4.929	4.9%



The average Error is 3.8%